Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A logic system for performing scan tests with a single scan clock comprising:

a first clock domain for performing logic operations and scan tests with a first clock signal;and

a second clock domain for performing logic operations with a second clock signal and for performing scan tests with the first clock signal;

wherein when the logic system performs scan tests, the first clock domain and the second clock domain have the clock tree quasi-balance characteristic.

[c2] 2.The logic system of claim 1 wherein the first clock domain further comprises at least one first-domain scan cell, the first-domain scan cell comprising:

a multiplexer for selectively outputting a function input signal or a scan input signal according to a scan enable signal; and

a D-type flip flop coupled to the multiplexer for receiving and outputting the function input signal or the scan input signal according to the first clock signal.

[c3] 3.The logic system of claim 1 wherein the second clock

domain further comprises:
a multiplexer for selectively outputting the first clock signal or the second clock signal as a second clock domain driving signal according to a mode signal; and
at least one second-domain scan cell comprising:
a multiplexer for selectively outputting a function input signal or a scan input signal according to a scan enable signal; and
a D-type flip flop coupled to the multiplexer for receiving and outputting the function input signal or the scan input signal according to the second clock domain driving signal.

[c4] 4.The logic system of claim 1 wherein when performing scan tests, the first clock domain and the second clock domain are linked to form a scan chain.

[c5] 5.The logic system of claim 1 wherein the second clock domain further comprises at least one second-domain scan cell comprising:
a first multiplexer for selectively outputtinga function input signal or a scan input signal according to a scan enable signal;
a second multiplexer for selectively outputting the first clock signal or the second clock signal according to a mode signal; and
a D-type flip flop coupled to the first multiplexer and the

second multiplexer for receiving and outputting the function input signal or the scan input signal according to the first clock signal or the second clock signal.

[c6] 6.A method for performing scan tests of a logic system, the logic system comprising a multiple clock domain scan test circuit having a first clock domain and a second clock domain, the method comprising:
when the logic system performs logic operations, performing logic operations according to a first clock signal and a second clock signal in the first clock domain and the second clock domain respectively; and
when the logic system performs scan tests, performing scan tests according to a test clock signal in both the first clock domain and the second clock domain so that the first clock domain and the second clock domain have the clock tree quasi-balance characteristic.

[c7] 7.The method of claim 6, wherein the test clock signal is the first clock signal.

[c8] 8.A scan cell for installation in a multiple clock domain scan chain circuit, the scan cell comprising:
a first multiplexer for selectively outputting a function input signal or a scan input signal according to a scan enable signal;
a second multiplexer for selectively outputting a first

clock signal or a second clock signal according to a mode signal; and

a D-type flip flop coupled to the first multiplexer and the second multiplexer for receiving and outputting the function input signal or the scan input signal according to the first clock signal or the second clock signal;

wherein when the multiple clock domain scan chain circuit performs logic operations, the first multiplexer outputs the function input signal and the second multiplexer outputs the first clock signal to the D-type flip flop; when the multiple clock domain scan chain circuit performs scan tests, the first multiplexer outputs the scan input signal and the second multiplexer outputs the second clock signal to the D-type flip flop.

[c9] 9.The scan cell of claim 8 wherein the multiple clock domain scan chain circuit comprises a plurality of linked scan cells, the output signal of a previous scan cell being the scan input signal of a next scan cell.

[c10]